## What is claimed is:

- 1. An apparatus for a compression architecture utilizing internal cache residing in main memory, the main memory comprising:
- 5 a compression cache to store a plurality of uncompressed data;
  - a compressed memory to store a plurality of compressed data; and
  - a compressed memory pointer table (CMPT) to store a plurality of pointers.
  - 2. The apparatus of claim 1 wherein the compression cache is a sectored cache.

- 3. The apparatus of claim 1 wherein the compression cache has a plurality of associated tags that are incorporated within a memory interface coupled to the apparatus.
- 4. The apparatus of claim 1 wherein the plurality of pointers are to the plurality of compressed data based on a plurality of cache block addresses.
  - 5. The apparatus of claim 3 is coupled to a memory interface that comprises:
  - a victim buffer to store at least one the entry that has been evicted from the compression cache;
- a CMPT offset calculator to provide an offset relative to the start of the CMPT based on an actual address of the data being compressed
  - 6. The apparatus of claim 5 wherein the memory interface is incorporated within a

processor or a chipset.

7. The apparatus of claim 6 wherein the apparatus is incorporated within a memory controller hub (MCH) of the chipset.

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8. The apparatus of claim 5 wherein the entry is evicted based on a first in first out (FIFO) protocol.

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- 9. The apparatus of claim 1 wherein the CMPT stores the plurality of pointers to the plurality of compressed data sequentially based on memory address for which the data is compressed.
- 10. An apparatus for a memory interface comprising:
- a first cache to store a plurality of tags for a compression cache;

a victim buffer to store at least one the entry that has been evicted from the compression cache;

an offset calculator to provide an offset relative to the start for a Compressed Memory Pointer Table (CMPT) based on an actual address of a data being compressed; and

- a second cache to store a plurality of pointers for the CMPT.
- 11. The apparatus of claim 10 wherein the memory interface is incorporated within a processor or a chipset.

- 12. The apparatus of claim 11 wherein the apparatus is incorporated within a memory controller hub (MCH) of the chipset.
- 13. The apparatus of claim 10 wherein the entry is evicted based on a first in first out (FIFO) protocol.

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- 14. A method for operating an memory operation comprising:

  receiving a memory address for the memory operation;

  storing a plurality of compressed data in a main memory; and

  performing a tag match between the memory address and a first cache storing a plurality of tags for a compressed memory in the main memory.
- 15. The method of claim 14 further comprising accessing a plurality uncompressed data access from the compression cache is performed if the tag match resulted in a hit.
  - 16. The method of claim 14 further comprising locating a pointer and subsequently finding a compressed memory location based at least in part on the pointer if the tag match resulted in a miss for the memory operation for a read miss.
  - 17. The method of claim 14 further comprising compressing the data and storing it in a compressed memory location for the memory operation for a write

miss.

- 18. A system comprising:
- a processor; and
- 5 a main memory, coupled to the processor, with a
  - a compression cache to store a plurality of uncompressed data;
  - a compressed memory to store a plurality of compressed data; and
  - a compressed memory pointer table (CMPT) to store a plurality of pointers.
- 19. The system of claim 18 wherein the compression cache is a sectored cache.
  - 20. The system of claim 18 wherein the compression cache has a plurality of associated tags that are incorporated within a memory interface coupled to the apparatus.
- 15 21. The system of claim 18wherein the plurality of pointers are to the plurality of compressed data based on a plurality of cache block addresses.
  - 22. A system comprising:
  - a processor; and
- a memory interface, coupled to the processor, with a:
  - a first cache to store a plurality of tags for a compression cache;
  - a victim buffer to store at least one the entry that has been evicted from the compression cache;
  - an offset calculator to provide an offset relative to the start for a Compressed

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Memory Pointer Table (CMPT) based on an actual address of a data being compressed; and

a second cache to store a plurality of pointers for the CMPT.

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23. The system of claim 22 wherein the memory interface is incorporated within a processor or a chipset.

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- 24. The system of claim 23 wherein the apparatus is incorporated within a memory controller hub (MCH) of the chipset.
- 25. The system of claim 22 wherein the entry is evicted based on a first in first out (FIFO) protocol.
- 26. A system comprising:

a processor, coupled to a memory bridge, the memory bridge to comprise;

- a first cache to store a plurality of tags for a compression cache;
- a victim buffer to store at least one the entry that has been evicted from the compression cache;

an offset calculator to provide an offset relative to the start for a Compressed Memory Pointer Table (CMPT) based on an actual address of a data being compressed; and

a second cache to store a plurality of pointers for the CMPT and

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a main memory, coupled to the memory bridge, to comprise

- a compression cache to store a plurality of uncompressed data;
- a compressed memory to store a plurality of compressed data; and
- a compressed memory pointer table (CMPT) to store a plurality of pointers.

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- 27. The system of claim 26 wherein the compression cache is a sectored cache.
- 28. The system of claim 26 wherein the compression cache has a plurality of associated
- tags that are incorporated within a memory interface coupled to the apparatus.

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29. The system of claim 26 wherein the plurality of pointers are to the plurality of compressed data based on a plurality of cache block addresses.